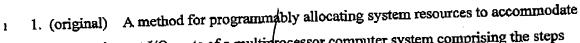
IN THE CLAIMS:



I/O transactions at I/O ports of a multiprocessor computer system comprising the steps

of:

determining the number and type of transactions anticipated at a port,

determining the number and type of devices being serviced via the port,

setting criteria for transactions at the port with respect to the number and type of

transactions and devices,

assigning the system resources to the port with respect to the criteria.

2. (original) The method as defined in claim 1 further comprising the steps of:

providing at least one control register for each port, wherein the control register 2

includes a plurality of programmable fields.

3. (original) The method as defined in claim 2 further comprising the steps of config-1

uring the control register fields to contain a number of direct memory access engines 2

available at a port to support a transaction, a number of cache lines for requested data, 3

and a number representing priorities among the anticipated transactions.

4. (original) The method as defined in claim 1 further comprising the step of preparing

for hot swapping an assembly, wherein the preparing for hot swapping comprises, with 2

respect to the assembly being replaced, copying the assembly's state, the state of its asso-3

ciated memory systems, its status and control registers, and the contents of its cache and

memory systems. 5

5. (original) The method as defined in claim 4 wherein the copying comprises the steps 1

of: 2

3	flushing the data in the local cache and local memory to storage not affected by
4	the hot swapping,
5	invalidating data in cache,
6	setting a flush indicator in the port's cache status and control register,
7	flushing directory data to non-affected storage,
. 8	finding and stopping any new transactions,
9	completing any transactions already started or pending,
10	flushing the translation look-aside buffers,
11	invalidating the contents of the translation look-aside buffers, and
12	updating the system directory.
1	6. (original) A system for allocating system resources to accommodate I/O transaction
2	at I/O ports of a multiprocessor computer system comprising:
3	the number and type of transactions anticipated at a port,
4	number and type of devices being serviced via the port,
5	criteria for operations at the port with respect to the number and type of transac-
6	tions and devices,
7	means for assigning the system resources to the port with respect to the criteria.
1	7. (original) The system as defined in claim 6 further comprising:
2	at least one control register for each port, wherein the control register includes a
3	plurality of programmable fields.
1	8. (original) The system as defined in claim 7 wherein the control register fields in-
2	
3	
4	among the anticipated transactions.
1	9. (previously presented) The method system as defined in claim 6 further compris
2	e ing:

3	means for hot swapping of an assembly, including means for copying the assem-
4	bly's state, the state of its associated memory systems, its status and control registers, and
5	the contents of its cache and memory systems.
1 2 3	10. (original) The system as defined in claim 9 wherein the means for copying comprises:: means for flushing the data in the local cache and local memory to storage not af-
4	fected by the hot swapping,
5	means for flushing, modifying and invalidating unmodified data in cache,
6	means for setting a flush indicator in the port's cache status and control register,
7	means for flushing directory data to non-affected storage,
8	means for finding and stopping any new transactions,
9	means for completing any transactions already started or pending,
10	means for flushing the translation look-aside buffers,
11	means for invalidating the contents of the translation look-aside buffers, and
12	means for updating the directory.
1 2 3 4	11. (previously presented) The method as defined in claim 1 herein the criteria comprises system needs with respect to operating speed, latency, priority, including low priority, debugging, communications credits, hot swapping, main and cache storage space, and control registers.
1	12. (previously presented) The system as defined in claim 6 wherein the criteria com
2	prises system needs with respect to operating speed, latency, priority, including low pri-
3	ority, debugging, communications credits, hot swapping, main and cache storage space,
4	and control registers.

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13. (new) A method for programmably allocating system resources to accommodate I/O transactions at I/O ports of a multiprocessor computer system comprising the steps

of: determining the number and types of transactions anticipated at a port, determining the number and types of devices being serviced via the port, 5 identifying assemblies for hot swapping, copying the states and status of those assemblies, copying the states and status of the memory systems associated with those assemblies, 9 copying the contents of control registers associated with those assemblies, 10 copying the contents of cache memories associated with those assemblies, 11 determining the operating speeds and latency for transactions at the port, 12 determining priority of transactions at the port, 13 in addition to the above, setting other criteria for transactions at the port with re-14 spect to the number and types of transactions and devices, and 15 with respect to the numbers and types of transactions and devices at the ports, as-16

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- 1 14.(new) The method as defined in claim 13 wherein the step of assigning system
 2 resources to the ports includes assigning control registers to the ports, assigning direct
 3 memory access engines to the ports, assigning cache memory to the ports and assigning
- memory access engines to the ports, assigning entered in priorities among the transactions at the ports.

signing system resources to the ports.

- 1 15. (new) A system for programmably allocating system resources to accommodate
- 2 I/O transactions at I/O ports of a multiprocessor computer system, the system comprising:
- means for determining the number and types of transactions anticipated at a port,

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	maans for	determining the numb	er and types of devices being serviced via the
4	means for	determine B	
5	port,		
6	assemblie	s identified for hot sw	apping,
7	means for	copying the states and	status of those assemblies,
8	means for	copying the states and	l status of the memory systems associated with
9	those asse	emblies,	
10	means fo	r control the contents	of registers associated with those assemblies,
11	means fo	r copying the contents	of cache memories associated with those assem-
12	blies,		
13	means fo	r determining the oper	ating speeds and latency for transactions at the
14	port,		
15	means fo	or determining priority	of transactions at the port,
16	in additi	on to the above, means	for setting other criteria for transactions at the por
17			f transactions and devices, and
18	with res	pect to the criteria, nur	hbers and types of transactions and devices at the
19		r assigning system reso	
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1 16.(new) The system as defined in claim 15 wherein the system resources assigned

to the ports includes control registers, direct memory access engines, cache memory and

means foe assigning priorities among the transactions at the ports.